Docket No.: 050432-0067 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 20277
Kai YANG, et al.	:	Confirmation Number: 9188
Application No.: 09/817,056	:	Group Art Unit: 2811
Filed: March 27, 2001	:	Examiner: T, NGUYEN

For: STABILIZING FLUORINE ETCHING OF LOW-K MATERIALS

TRANSMITTAL OF APPEAL BRIEF

Mail Stop Appeal Brief
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Submitted herewith in triplicate is Appellant(s) Appeal Brief in support of the Notice of Appeal filed July 22, 2005. Please charge the Appeal Brief fee of $500.00 to Deposit Account 500417.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due under 37 C.F.R. 1.17 and 41.20, and in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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APPEAL BRIEF

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Sir:

This Appeal Brief is submitted in support of the Notice of Appeal filed on July 22, 2005.

I. REAL PARTY IN INTEREST

The real part in interest is Advanced Micro Devices Inc.

II. RELATED APPEALS AND INTERFERENCES

Appellants are unaware of any related Appeal or Interference.

III. STATUS OF CLAIMS

Claims 1 through 23 are pending in this application. Claims 13 through 20 stand withdrawn from consideration pursuant to the provisions of 37 C.F.R. § 1.142(b). Claims 6

through 12 have been allowed. Claims 1 through 5 and 21 through 23 have been subject to repeated rejections. In fact, independent claim 1 has been rejected in no less than seven Office Actions, the most recent dated July 15, 2005. It is from the repeated rejection of claims 1 through 5 and 21 through 23 that this Appeal is taken.

IV. STATUS OF AMENDMENTS

No Amendment has been filed subsequent to the most recent Office Action dated July 15, 2005.

V. SUMMARY OF CLAIMED SUBJECT MATTER

Independent claim 1 is directed to a method of manufacturing a semiconductor device. The claimed method comprises forming a single first dielectric layer (Fig. 3; element 30) overlying a substrate (Fig. 3; element 13), forming a first barrier layer (Fig. 3; element 31) of a first dielectric material on the single first dielectric (30), and then etching to form a single opening (Fig.3; element 32) entirely within and defined by side surfaces (Fig. 3; elements 30A) of the single first dielectric layer (30) and a bottom over an underlying conductive feature (Fig. 3; element 20); (page 6 of the written description of the specification, lines 3 through 5). Subsequently, a second barrier layer (Fig. 4; element 40) is deposited on the first barrier layer (31) and on the side surfaces of the first dielectric layer (30), and etching is conducted to remove the second barrier layer (40) from and stopping on the upper surface of the first barrier layer (31) and to remove the second barrier layer (40) from the bottom of the single opening, thereby exposing the underlying conductor feature (20) leaving a portion of the second barrier layer (Fig. 5; element 50) as a liner on the side surfaces of the single first dielectric layer (30); (page 6 of the written description, lines 5 through 14). The opening (32) is then filled with metal forming an

overburden and then planarized to form a lower metal feature (Fig. 6; element 60); (page 6 of the written description, lines 19 through 22).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1 through 5 and 21 through 23 stand rejected under 35 U.S.C. § 103 for obviousness predicated upon Chooi et al. in view of Lou and Chung et al.

VII. ARGUMENT

For the convenience of the Honorable Board of Patent Appeals and Interferences (the "Board"), Applicants only separately argue the patentability of independent claim 1. Accordingly, all of the appealed claims, claims 1 through 5 and 21 through 23, stand or fall together with independent claim 1.

The Examiner's Position.

Although the claimed invention is clearly directed to a **single** damascene technique, the Examiner's primary reference to Chooi et al. is confined to a **dual** damascene technique. As one having ordinary skill in the art would have understood, a single damascene technique comprises forming a via or contact hole or a trench in a single dielectric layer, which opening is subsequently filled with metal. On the other hand, a dual damascene technique comprises both a via or contact hole and an overlying trench, typically in two dielectric layers. When the dual damascene opening is filled with metal, a lower via or contact connected to an upper metal line are simultaneously formed.

The Examiner's primary reference to Chooi et al. involves a dual damascene technique. In other words, the methodology disclosed by Chooi et al. does not comprise various

manipulative steps of the claimed invention. For example, the Examiner's determinations notwithstanding, the method disclosed by Chooi et al. does not comprise forming a **single** opening entirely within and defined by side surfaces of a **single** first dielectric layer and with a bottom **over** an underlying feature. In addition, the method disclosed by Chooi et al. does not comprise etching with selectivity to the first barrier layer to remove the second barrier layer from the **bottom** of the single opening thereby **exposing** the underlying metal feature. The Examiner's secondary reference to Chung et al. is merely relied upon for the notion of forming a silicon nitride capping layer by CVD, which is not an issue in this Appeal.

The Examiner attempts to bridge the chasm between the claimed single damascene method and the dual damascene method of Chooi et al. by pointing out that Lou discloses the formation of both single and dual damascene techniques. The Examiner would then disregard the **particular techniques** disclosed by each of Chooi et al. and Lou, asserting that the difference between a single damascene technique or a dual damascene technique is a "design choice", as though that rubric **automatically** provides the requisite fact-based motivation without any further reasoning in defiance of consistent legal precedent. Appellants, of course, disagree.

Appellants' Position

That single and dual damascene techniques are known in general cannot be gainsaid. But the issue is not what may or may not be known in general. The issue is whether the Examiner provided the requisite factual basis to support the conclusion that one having ordinary skill in the art would somehow have been realistically motivated to modify the **particular** methodology of Chooi et al by converting the dual damascene technique into a single damascene technique and then to conduct that single damascene technique specified in the claimed invention. *Teleflex Inc.*

v. Ficosa North America Corp., 299 F.3d 1313, 63 USPQ2d 1374. Appellants submit the Examiner did not discharge that initial burden and, hence, did not establish a *prima facie* case.

Appellants stress that the method disclosed by Chooi et al., does not comprise forming **single** opening **entirely** within and defined by side surfaces of a **single** first dielectric layer and a bottom over an underlying conductive feature. This is because Chooi et al. etch to form a **dual-damascene opening** within **two** dielectric layers. The Examiner improperly rewires the invention disclosed by Chooi et al. by partitioning the dual damascene opening formed by Chooi et al. into separate upper and lower openings. But the Examiner is not free to rewrite the applied prior art. There is only **one opening** formed by Chooi et al. and it is in **two** dielectric layers, **not entirely in one dielectric layer as claimed**.

The Examiner says but does **not** identify wherein Chooi et al. etch to form a single opening entirely within the first dielectric layer and a bottom over an underlying conductor feature – **because he cannot**. The Examiner says that what the single opening (22) is entirely within the first dielectric layer 18 and has a bottom. Where is that bottom? The bottom of the opening disclosed in Fig. 1 of Chooi et al. is over an underlying conductive feature, but that bottom penetrates a **second** dielectric layer 14 and is **not** entirely within the first dielectric layer 18.

There is no motivation

The Examiner is of the opinion that the rubric "design choice" automatically establishes the requisite motivation to **dramatically modify** the methodology of Chooi et al. to arrive at the claimed invention. But the Examiner's reasoning is clearly legally erroneous. *In re Chu, 66*

F.3d 292, 36 USPQ2d 1089 (Fed. Cir. 1995); In re Gal, 980 F.2d 717, 25 USPQ2d 1076 (Fed. Cir. 1992); In re Bezombes, 420 F.2d 1070, 164 USPQ 387 (CCPA 1970).

As previously acknowledged, single and dual damascene techniques are known. But it does not follow that one having ordinary skill in the art would have been realistically motivated to convert every dual damascene technique into a single damascene technique.

The Examiner's allegedly teaching reference discloses a **particular** dual damascene technique. That particular technique involves lining the dual damascene opening with a diffusion barrier layer. Nitride spacers are then formed on the inside walls of both the trench opening and the via opening. The via opening is further lined with a displacement layer or seed layer. Electroless copper is then deposited and then a copper plug. A barrier metal is then formed over the copper plug and the inside walls of the trench opening. Copper is then deposited over the barrier metal inside the trench and over the cooper metal plug using physical vapor deposition. The Examiner seizes upon an evulgation appearing in column 7 of Lou, lines 34 through 38, that same approach can be applied to not only dual damascene **structures** but also to single damascene **structures**. But Lou does not teach conversion of every dual-damascene **technique** into a single damascene **technique**. Lou teaches that the particular disclosed **structure** can be formed as both a single damascene **structure** and dual damascene **structure**. The Examiner did not provide any factual basis upon which to predicate the conclusion that one having ordinary skill in the art with Lou in hand would automatically have assumed that any dual-damascene **technique** vis-à-vis **structure** can be converted into a single damascene technique, let alone the particular technique of Chooi et al.

Indeed, it is inconceivable that one having ordinary skill in the art would have been realistically led to modify the **particular methodology** of Chooi et al. by converting the dual

damascene technique into a single damascene technique. Appellants submit the Examiner did **not** even establish that the formation of a single damascene technique is **consistent** with the **objective** of Chooi et al. *In re Fitch, 972 F.2d 1260, 23 USPQ2d 1780 (Fed. Cir. 1992); In re Gordon, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984); In re Schulpen, 390 F.2d 1009, 157 USPQ 52 (CCPA 1968).*

Appellants respectfully invite the Honorable Board's attention to Fig. 1 of Chooi et al., which is the starting point for the disclosed method. The Examiner did not provide a factual basis upon which to conclude that one having ordinary skill in the art would have been realistically led to dramatically modify the disclosed dual damascene technique by converting it into a single damascene technique. *Ecolochem Inc. v. Southern California Edison, Co. 227 F.3d 1361, 56 USPQ2d 1065 (Fed. Cir. 2000); In re Kotzab, 217 F.3d 1365, 55 USPQ 1313 (Fed. Cir. 2000); In re Dembiczak, 175 F.3d 994, 50 USPQ2d 1614 (Fed. Cir. 1999); In re Rouffet, 149 F.3d 1350, 47 USPQ2d 1453 (Fed. Cir. 1998).*

Moreover, the Examiner does not even explain **how** a single damascene technique would be implemented to achieve the objective of Chooi et al. if, indeed, it can. The Examiner leaves it to the **imagination** of the reader **how** to convert the dual damascene technique of Chooi et al. into a single damascene technique, and then to somehow select appropriate pieces to arrive at the claimed invention. This approach flies in the face of consistent judicial precedent requiring facts and reasons. *Ecolochem Inc. v. Southern California Edison, Co., supra; In re Kotzab, supra; In re Dembiczak, supra; In re Rouffet, supra.*

Conclusion

Appellants submit that the Examiner failed to proffer the requisite factual basis to support the conclusion that one having ordinary skill in the art would have been realistically motivated to modify the particular methodology of Chooi et al. by converting the disclosed dual damascene technique into a single damascene technique, let alone in such a manner to somehow arrive at the claimed invention. The Examiner, therefore, failed to establish a *prima facie* case of obviousness under 35 U.S.C. §103.

Appellants, therefore, submit that the Examiner's rejection of claims 1 through 5 and 21 through 23 under 35 U.S.C. § 103 for obviousness predicated upon Chooi et al. in view of Lou and Chung et al. is not factually or legally viable.

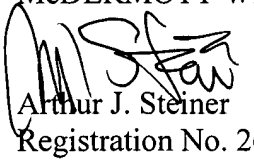
VIII. PRAYER FOR RELIEF

Based upon the arguments submitted *supra*, Appellants submit that the Examiner's rejection of claims 1 through 5 and 21 through 23 under 35 U.S.C. § 103 is not factually or legally viable. Appellants, therefore, solicit the Honorable Board to reverse the Examiner's rejection of the appeal claims under 35 U.S.C. § 103.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP



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Please recognize our Customer No. 20277 as our correspondence address.

CLAIMS APPENDIX

1. A method of manufacturing a semiconductor device, the method comprising:

forming a single first dielectric layer overlying a substrate;

forming a first barrier layer, comprising a first dielectric barrier material, on the single first dielectric layer with an interface therebetween,

etching to form a single opening entirely within and defined by side surfaces of the single first dielectric layer and a bottom over an underlying conductive feature;

forming a second barrier layer, comprising a second dielectric barrier material different from the first dielectric barrier material, on and in contact with an entire upper surface of the first barrier layer overlying the single first dielectric layer, on the side surfaces of the single first dielectric layer defining the single opening and on the bottom of the single opening;

etching, with selectivity to the first barrier layer, to remove the second barrier layer from, and stopping on, the upper surface of the first barrier layer, and to remove the second barrier layer from the bottom of the single opening exposing the underlying conductive feature, leaving a portion of the second barrier layer as a liner on the side surfaces of the single first dielectric layer defining the single opening;

filling the single opening with metal forming an overburden on the first barrier layer; and

planarizing to form a lower metal feature.

2. The method according to claim 1, wherein the first and second dielectric barrier materials are selected from the group consisting of silicon nitride, silicon oxynitride and silicon carbide.

3. The method according to claim 2, comprising depositing each of the first and second barrier layers by chemical vapor deposition.

4. The method according to claim 3, comprising depositing each of the first and second barrier layers at a thickness of about 50Å to about 500Å.

5. The method according to claim 1, comprising filling single opening with copper (Cu) or a Cu alloy.

21. The method according to claim 1, comprising etching to form the single opening having entire side surfaces which are substantially parallel.

22. The method according to claim 1, comprising etching to remove the second barrier layer leaving a portion of the second barrier as a liner on the side surfaces of the single first dielectric layer with a gap between an upper surface of the liner and an upper surface of the first barrier layer.

23. The method according to claim 22, wherein the gap is about 50Å to about 500Å.